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The CAT5132 Used for V_{COM} Buffer Control in a TFT LCD Display

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APPLICATION NOTE

Application Overview

All TFT (thin−film−transistor) LCD panels require at least one appropriately tuned V_{COM} signal to provide a reference point for the panel's back plane (or back plate). Figure 1 is a simplified block diagram to provide the relationship of the V_{COM} inputs within an LCD panel with other inputs. The exact value of V_{COM} varies from panel to panel, so the manufacturer must program the voltage at the factory to match the characteristics of each screen. An appropriately tuned V_{COM} value reduces flicker and other undesirable effects.

Solution History

Traditionally, the V_{COM} adjustment made use of mechanical potentiometers or trimmers (see Figure 2) in the voltage−divider mode. In recent years, however, panel makers have begun looking at alternative approaches because inexpensive mechanical trimmers don't provide the manufacturing ease and desired reliability. The physical adjustment process on the assembly line also leads to inconsistent results from display to display. This adjustment is not only time−consuming, but also prone to field failures arising from human error and mechanical vibration. Additionally low cost mechanical potentiometers tended to be more vulnerable to environmental degradation over time causing long term reliability issues.

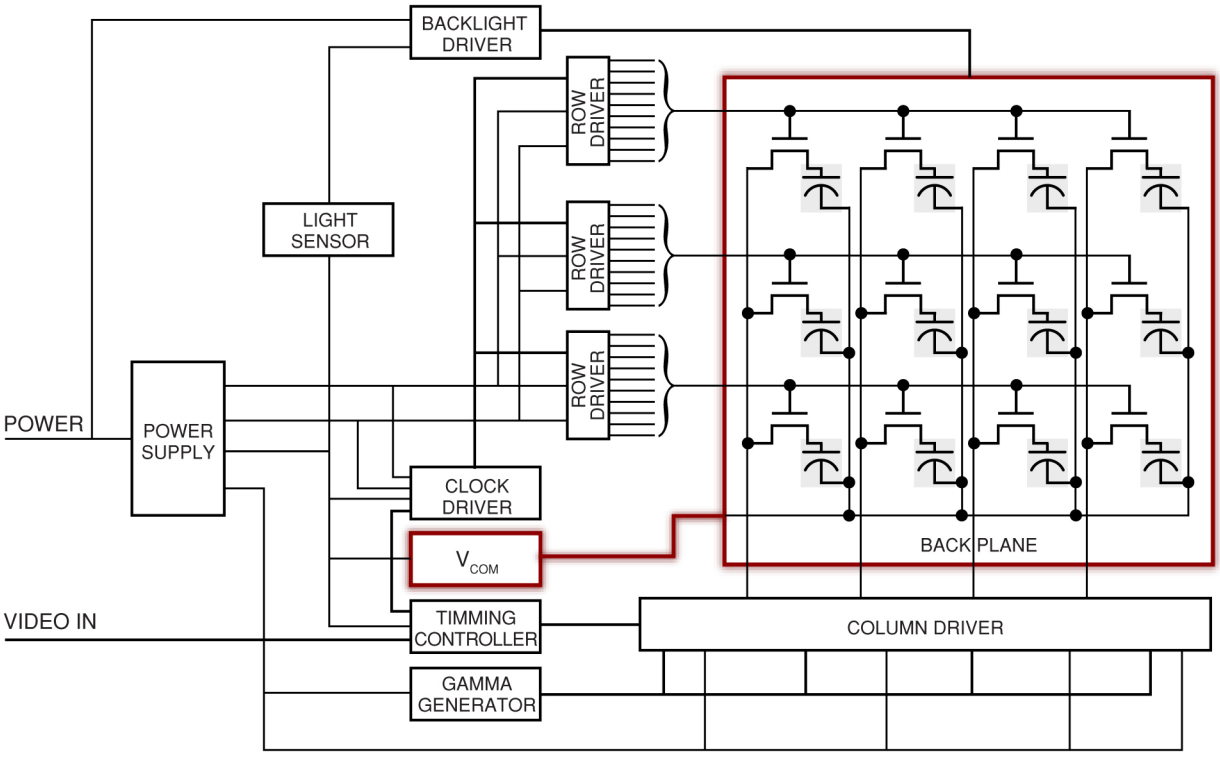

Figure 1. Simplified Block Diagram of a TFT−LCD Display

The issues with the mechanical potentiometer solution lead vendors to seek an all silicon solution with the most obvious being to replace the mechanical potentiometer with a DAC as shown in Figure 3. This solution solved the problem of the degradation over time but was expensive. Not only did the DAC have to be very high resolution to deal with the fact that the DAC output was 0 V to 5 V and typically required a gain stage Op Amp in many circumstances to cover all the possible output ranges. Because DAC's are volatile they also required some form of direct control to set the output voltage after the display is powered on. This causes the system start up to be complex and time consuming.

The use of a nonvolatile digital potentiometer would address the issues with both of the above solutions. Because digital potentionmeters have a serial bus input, they allow panel makers to automate the V_{COM}−adjustment process, resulting in lower manufacturing costs and higher product reliability. Additionally, since they are silicon devices like a DAC, they are not affected by typical environmental issues and provide a very long life expectancy. Unlike a DAC however, using a resistive device with high voltage capabilities creates two additional advantages 1) a gross calibration can be achieved by the use of inexpensive external resistors putting the bits of resolution exactly where truly required, and 2) the high voltage capability removes the requirement for a gain stage Op Amp which reduces system noise.

The CAT5132 high voltage/nonvolatile digital potentiometer (Block Diagram shown in Figure 4) overcomes the complaints discussed above with mechanical potentiometers and DAC's. The CAT5132 is a 7 bit (128 position) all silicon potentiometer with a nonvolatile memory and capable of resistor terminal voltages as high as 16 V. The CAT5132 solution maintains the simplicity of the mechanical potentiometer solution while providing the versatility and reliability of the DAC solution at a much lower cost. Shown with a controller in Figure 5. The controller would only be required for the calibration process and would be omitted for normal operation.

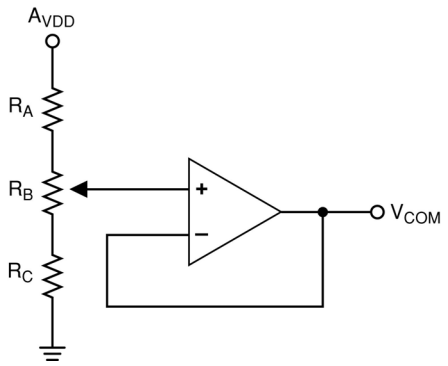

Figure 2. Typical Mechanical Potentiometer V_{COM} Solution with Op Amp in the Voltage Follower/Buffer configuration

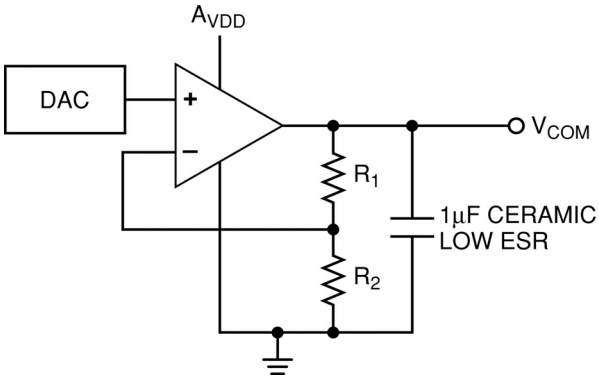

Figure 3. Typical DAC Implementation with an Op Amp Used as a Gain Stage/buffer

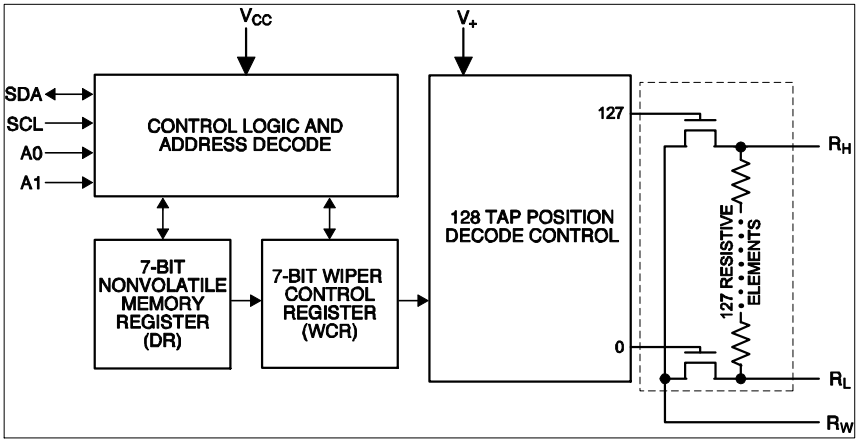

Figure 4. CAT5132 Block Diagram

The system implementation for a V_{COM} calibration with a CAT5132 is straightforward as shown in a typical application Figure 5. Resistors shown in Figure 5 (R1 and R3) can be adjusted to meet the specific needs of the display being adjusted but the basic circuit would be as shown. The Op Amp simply acts as a buffer for the variations in current required on the display back plane while the 1 μF capacitor provides short duration current requirements. An I^2C serial interface provides control and stores the desired potentiometer setting into the EEPROM. The 10 pin MSOP package also provides a small foot print to minimize space and removing the physical access for a manual adjustment can dramatically improve board layout efficiency for today's space−constrained designs.

Solution Implementation

The CAT5132 has a V_{CC} pin that is connected to any available logic supply. V_{CC} is 2.7 to 5.5 V and draws a maximum of 5 μA except during a nonvolatile write when it can draw up to 3mA. The analog input V+ draws a maximum of 10 μA and is designed to be directly supplied from +8 to +16 V to bias the wiper switches in the digital potentiometer's resistor string. If a panel requires a V_{COM} voltage greater than 16 V, the op amp could still be used in a non−inverting gain configuration however with a lower gain, noise will still be less than with an equivalent DAC solution.

The digital potentiometer has a maximum ±20% end−to−end resistor tolerance. The results in Table 1 show what could be expected using the circuit shown in Figure 5. It assumes that the tolerances of R1, R3, and V_{DD} are negligible compared with those of the potentiometer; you can expect the range of output values indicated. The desired value used for this example was V_{COM} at 7.2 V ±0.5 V, with a step size of approximately 10 mV. The value R2 would be the value of the CAT5132 wiper to low potentiometer terminal minus the wiper resistance. The wiper resistance would have minimal impact in this voltage divider configuration driving a high impedance Op Amp input. And, despite the ±20% tolerance of R2, the midscale V_{COM} output meets the target specification. Also, because the digital potentiometer's logic supply matches the microcontroller's logic levels, the microcontroller can read the position data back if desired.

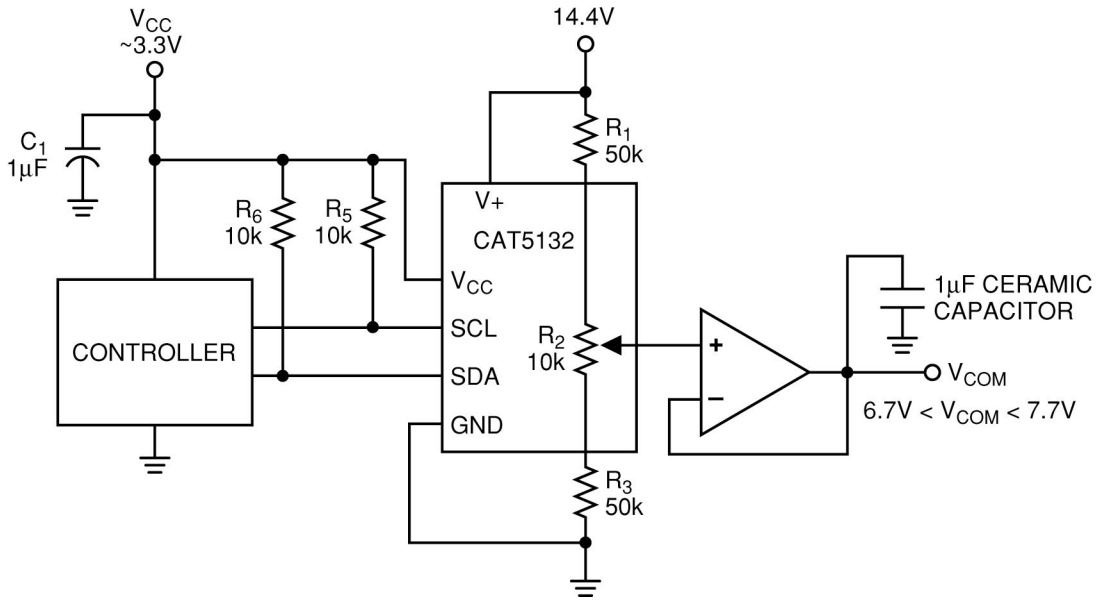

Figure 5. Typical Application Using the CAT5132

Table 1. OUTPUT VOLTAGE RANGE

R2 Tolerance, Scale	R2 (kΩ)	V_{COM} (V)	Step Size (mV)
−20%, Zero	0	6.65	8.3
−20%, Mid	4	7.18	
−20%, Full	8	7.71	
+20%, Zero	0	6.45	12.1
+20%, Mid	6	7.22	
+20%, Full	12	8.00	

NOTE: The value R_2 used in this table is the value of the CAT5132 wiper to the low terminal minus the wiper resistance.

Calculations for Table 1:
Know Values:

Analog Voltage = 14.4 V

$R_1 + R_2 + R_3 = R_{total}$

Minimum DPP™ Resistance = 8 kΩ Maximum DPP Resistance = 12 kΩ

External Resistors = 50 kΩ each

1. **Determine total series resistance**

Formula:

$R_1 + R_2 + R_3 = R_{total}$

Minimum total series resistance:
50 kΩ + 8 kΩ + 50 kΩ = 108 kΩ

Maximum total series resistance:
50 kΩ + 12 kΩ + 50 kΩ = 112 kΩ

2. **Determine current through the resistive channel**

Formula:

$$\frac{\text{Analog Voltage}}{\text{Total Resistance}} = \text{Current}$$

Minimum Resistance Current:

$$\frac{14.4\ \text{V}}{108\ \text{k}\Omega} = 133\ \mu\text{A}$$

Maximum Resistance Current:

$$\frac{14.4\ \text{V}}{112\ \text{k}\Omega} = 129\ \mu\text{A}$$

3. **Determine Voltages at the output of the DPP**

Formula:

$$\text{Current} * \text{Resistance} = \text{Voltage}$$

Minimum DPP Resistance Calculations @ Wiper output:

Minimum Voltage	Middle Voltage	Maximum Voltage
133 μA * 50 kΩ = 6.65 V	133 μA * 54 kΩ + 7.18 V	133 μA * 58 kΩ + 7.71 V

Maximum DPP Resistance Calculations @ Wiper output:

Minimum Voltage	Middle Voltage	Maximum Voltage
129 μA * 50 kΩ = 6.45 V	129 μA * 56 kΩ + 7.22 V	129 μA * 62 kΩ + 8.00 V

4. **Determine LSB step voltage**

Formula:

$$\frac{V_{FULL} - V_{Zero}}{\#\ \text{of Steps}} = \text{Voltage Step}$$

Step Size DPP Minimum Resistance:

$$\frac{7.71\ \text{V} - 6.65\ \text{V}}{128} = 8.3\ \text{mV}$$

Step Size DPP Maximum Resistance:

$$\frac{8.00\ \text{V} - 6.45\ \text{V}}{128} = 12.1\ \text{mV}$$

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